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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,782	11/05/2003	Ronald Patrick Huemoeller	W0308039	7434
23504	7590	02/08/2006	EXAMINER	
WEISS & MOY PC 4204 NORTH BROWN AVENUE SCOTTSDALE, AZ 85251				SEMENENKO, YURIY
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,782	HUEMOELLER ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 December 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 and 21-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-18 and 21-22 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 05 November 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8/15/5;6/9/5;1/31/05,
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Restriction election

1. Applicant's election of Group I and Group III claims 1-18 drawn to a substrate and an integral ceramic circuit board in the reply filed on 12/16/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim 19-20 has been cancelled. Claims 21-22 are newly added.

Claims 1-18 and 21-22 are now pending in the application.

Specification

2.1. Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

2.2 The disclosure is objected to because of the following informalities:

2.2.1. There is not grid 28A in Fig. 3A, as discloses in page 13

2.2.2. There are not Die 26B, substrate 10C in Fig. 5B, as discloses in page 14

Appropriate correction is required.

Claim Objections

3. Claims 10 and 14 objected to because of the following informalities:

Claims 10 and 14 claimed "The integrated circuit" and depend on claim 1 which claimed "a substrate".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 9 and 17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite: It is unclear whether the function of “plating and etching current density of the circuit material deposited within the at least one land area is reduced and dimpling of the circuit material within the at least one land area is reduced or eliminated.” requires a particular shape (or means) and such shape (means) is not already, recited in the claim (and in that case, examiner is unsure what shape (means) is being claimed) or whether the function results from the already recited claim structural limitations. To apply art, examiner assumed that the functionality follow from the already recited structure (MPEP 2114).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.1. Claims 1-4, 6-12, 14-18, 21 and 22 are rejected under 35U.S.C. 103(a) as being obvious over Gebhardt et al. (Patent #5928767) hereinafter Gebhardt in view of Takeuchi et al. (Patent #5744224) hereinafter Takeuchi.

As to claims 1, 9 and 17 Gebhard discloses in Fig.4 and 6 a substrate 80 for mounting at least one die 85a within an integrated circuit (column 57, lines 18-21), comprising: dielectric layer 6 (column 54, lines 51-65) defining a first surface of the substrate, Fig.4a, and having channels therein for addition of circuit material 84, 86, 93 (column 56, lines 39-42), the channels Fig. 6a, b having sides extending to a plane defining the first surface of the substrate and having a bottom beneath the plane defining the first surface of the substrate, and wherein the channels include at least one land area formed from multiple channels (land on intersection of channels (grooves) 93 and 84 within the substrate 80; and circuit material 5', Fig. 1b deposited within the channels for forming an electrical connection between electrical contacts of the at least one die 85a and electrical terminal lands on the substrate,

except, Gebhardt doesn't explicitly teach the at least one land area forms a shape having non-channel regions within a perimeter of the land area.

Takeuchi discloses in Fig. 1 the at least one land area 10 forms a shape having non-channel regions 12 within a perimeter of the land area 10.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Gebhardt include in his invention that the at least one land area forms a shape having non-channel regions within a perimeter of the land area, as taught by Takeuchi because Takeuchi teaches that such a configuration would result in the benefit of a thermal stress does not appear (column 2, lines 29-32).

Instant Gebhard, as modified, clearly teaches the Applicant's claimed "at least one land area formed from multiple channels" and "one land area forms a shape having non-channel regions within a perimeter of the land area" structures. However, the examiner notes that a limitation " plating and etching current density of the circuit material deposited within the at least one land area is reduced and dimpling of the circuit material within the at least one land area is reduced or eliminated" are a process limitations in the product claim. Such a process limitations define the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

As to claims 2, 3,10, 11,18 and 21 Gebhardt, as modified, discloses everything, as discussed above with respect of claim 1, 9 and 17,

except, Gebhardt does not teach the at least one land area is a grid formed from multiple channels within the perimeter of the at least one land area, whereby the circuit material deposited within the perimeter of the at least one land area forms a grid of conductive material as claimed claim 2 (10, 18, 21), and the multiple channels comprise: a first plurality of parallel channels; a second plurality of parallel channels orthogonal to the first plurality of parallel channels in a plane defined by the first surface of the substrate, as claimed claim 3 (11).

Takeuchi discloses in Fig. 1 the at least one land area 10 is a grid formed from multiple channels 14 within the perimeter of the at least one land area 10, whereby the circuit material deposited within the perimeter of the at least one land area forms a grid of conductive material as claimed claim 2 (10, 18,21), and the multiple channels comprise: a first plurality of parallel channels; a second plurality of parallel channels orthogonal to the first plurality of parallel channels in a plane defined by the first surface of the substrate, as claimed claim 3 (11). [As shown on Fig. 1 each channel 14 has portion of the channel parallel to and orthogonal to a corresponding portion of the

another channels in a plane defined by the first surface of the substrate and such satisfied to claim 3.]

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Gebhardt include in his invention that the at least one land area is a grid formed from multiple channels within the perimeter of the at least one land area, whereby the circuit material deposited within the perimeter of the at least one land area forms a grid of conductive material as claimed claim 2 (10, 18, 21), and the multiple channels comprise: a first plurality of parallel channels; a second plurality of parallel channels orthogonal to the first plurality of parallel channels in a plane defined by the first surface of the substrate, as claimed claim 3 (11) , as taught by Takeuchi because Takeuchi teaches that such a configuration would prevent a deformation or a curvature of the chip, column 3, lines 52-54). And more such grid will reduce a plating area of the land.

As to claims 4 and 12 Gebhardt, as modified, discloses substrate, having all of the claimed features as discussed above with respect claim 2 (10),

except, Gebhardt does not teach the perimeter of the at least one land area is a rectangle, whereby a mounting land for a surface-mount component is provided by the circuit material deposited within the at least one land area.

Takeuchi discloses in Fig. 4 the perimeter of the at least one land area is a rectangle, whereby a mounting land for a surface-mount component is provided by the circuit material deposited within the at least one land area. Although Takeuchi teaches rectangle shape of pad for chip component such pads can be used without modifications for surface-mount component.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Gebhardt include in his invention that the perimeter of the at least one land area is a rectangle, whereby a mounting land for a surface-mount component is provided by the circuit material deposited within the at least one land area to provide robust electrical connection for surface-mount component.

As to claims 6-8, 14-16 and 22 Gebhardt, as modified, discloses substrate, having all of the claimed features as discussed above with respect claim 1 (9, 17),

except, Gebhardt does not teach the at least one land area is multiple channel sub-areas having a common predetermined geometric shape and disposed radially around center of the at least one land area, and further comprising interconnect channels interconnecting the multiple channel sub-areas, whereby the circuit material deposited within the perimeter of the at least one land area forms a circular pattern having voids between the sub-areas, and one of the sub-areas is first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are circular areas radially disposed around the first circular sub-area, and one of the sub-areas first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are annular segments radially disposed around the first circular sub-area.

Takeuchi discloses in Fig. 3 the at least one land area 10 is multiple channel sub-areas [sub-areas in Fig. 3 are separated by voids 12] having a common predetermined geometric shape 16 and disposed radially around center of the at least one land area, and further comprising interconnect channels interconnecting the multiple channel sub-areas, whereby the circuit material deposited within the perimeter of the at least one land area forms a circular pattern having voids 12 between the sub-areas, as claimed claim 6 (14), and one of the sub-areas is first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are circular areas radially disposed around the first circular sub-area, as claimed claim 7 (15), and one of the sub-area is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are annular segments radially disposed around the first circular sub-area, as claimed claim 8,(16) (please see Fig. 3).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Gebhardt include in his invention that the at least one land area is multiple channel sub-areas having a common predetermined geometric shape and disposed radially around center of the at least one land area, and further comprising interconnect channels interconnecting the multiple channel sub-areas,

whereby the circuit material deposited within the perimeter of the at least one land area forms a circular pattern having voids between the sub-areas, as claimed claim 6 (14), and one of the sub-areas is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are circular areas radially disposed around the first circular sub-area, as claimed claim 7 (15) and one of the sub-area is first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are annular segments radially disposed around the first circular sub-area, as claimed claim 8 (16), as taught by Takeuchi, because Takeuchi teaches that such a configuration would result in the benefit of a thermal stress does not appear (column 2, lines 29-32).

5.2. Claims 5 and 13 are rejected under 35U.S.C. 103(a) as being obvious over Gebhardt in view of Takeuchi and Edwards et al. (Patent #6064576) hereinafter Edwards.

As to claims 5 and 13 Gebhardt, as modified, discloses substrate, having all of the claimed features as discussed above with respect claim 2 (10),

except, Gebhardt does not teach the perimeter of the at least one land area is a circle, whereby a land for a solderball is provided by the circuit material deposited within the at least one land area.

Takeuchi discloses in Fig. 3 the at least one land area is included a circle, whereby a land is provided by the circuit material deposited within the at least one land area. Although Takeuchi does not explicitly teaches the perimeter of the at least one land area is a circle, and a land is the land for a solderball at time the invention was made, it was well known to make shape of the land for solderball as a circle (Please see Edwards , Fig.3).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Gebhardt include in his invention that the perimeter of the at least one land area is a circle, whereby a land for a solderball is provided by the circuit material deposited within the at least one land area.

Circle' shape provides reducing of a plating area of the land.

Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rinne et al. (Patent # 6388203) discloses lot of different shapes of lands (bumps).

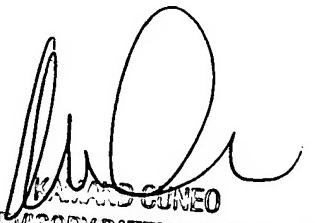
Christiansen (Patent #3833838) discloses wafers with a multiplicity of sets of electrically conducting pads.

7.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

7.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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